S.N.: 10/720,585 Art Unit: 2181

## **AMENDMENTS TO THE SPECIFICATION:**

Please replace the paragraph beginning on line 3 of page 13, with the paragraph below. No new matter is added.

In the embodiment of Fig. 4 the MUX 13B is eliminated, and the output of the code page 12 is applied directly to the fetch stage 20, via the 32-bit original instruction bus 13A and via an 8-bit extended instruction bus 13C. In this embodiment the decode stage 22 of the instruction pipeline is controlled by the Ext\_Ins\_Page PTE bit to either ignore or decode the eight extension bits, on a page-by page basis, and the combination of the 32-bit instruction and the 8-bit extension is thus performed in the fetch stage 20 and selectively in the decode stage 22.

In the embodiment of Fig. 4 the MUX 13B is eliminated, and the output of the code page 12 is applied directly to the fetch stage 20, via the 32-bit original instruction bus 13A and via an 8-bit extended instruction bus 13C. In this embodiment the decode stage 22A of the instruction pipeline is controlled by the Ext\_Ins\_Page PTE bit to either ignore or decode the eight extension bits, on a page-by-page basis, and the combination of the 32-bit instruction and the 8-bit extension is thus performed in the fetch stage 20 and selectively in the decode stage 22A.